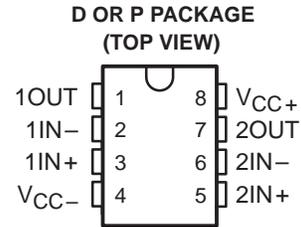


- Low Input Bias Current . . . 50 pA Typ
- Low Input Noise Current
0.01 pA/√Hz Typ
- Low Input Noise Voltage . . . 18 nV/√Hz Typ
- Low Supply Current . . . 3.6 mA Typ
- High Input Impedance . . . 10¹² Ω Typ
- Internally Trimmed Offset Voltage
- Gain Bandwidth . . . 3 MHz Typ
- High Slew Rate . . . 13 V/μs Typ



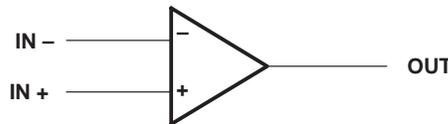
description

This device is a low-cost, high-speed, JFET-input operational amplifier with very low input offset voltage. It requires low supply current yet maintains a large gain-bandwidth product and a fast slew rate. In addition, the matched high-voltage JFET input provides very low input bias and offset currents.

The LF353 can be used in applications such as high-speed integrators, digital-to-analog converters, sample-and-hold circuits, and many other circuits.

The LF353 is characterized for operation from 0°C to 70°C.

symbol (each amplifier)



AVAILABLE OPTIONS

T _A	V _{IO} max AT 25°C	PACKAGE	
		SMALL OUTLINE (D)	PLASTIC DIP (P)
0°C to 70°C	10 mV	LF353D	LF353P

The D packages are available taped and reeled. Add the suffix R to the device type (ie., LF353DR).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} +	18 V
Supply voltage, V _{CC} -	-18 V
Differential input voltage, V _{ID}	±30 V
Input voltage, V _I (see Note 1)	±15 V
Duration of output short circuit	unlimited
Continuous total power dissipation	500 mW
Operating temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply voltage.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



LF353
JFET-INPUT
DUAL OPERATIONAL AMPLIFIER
 SLOS012B – MARCH 1987 – REVISED AUGUST 1994

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC+}	3.5	18	V
Supply voltage, V_{CC-}	-3.5	-18	V

electrical characteristics over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V (unless otherwise specified)

PARAMETER		TEST CONDITIONS	T_A^\dagger	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = 0, R_S = 10 \text{ k}\Omega$	25°C		5	10	mV
			Full range			13	
α_{VIO}	Average temperature coefficient of input offset voltage	$V_{IC} = 0, R_S = 10 \text{ k}\Omega$			10		$\mu\text{V}/^\circ\text{C}$
I_{IO}	Input offset current \ddagger	$V_{IC} = 0$	25°C		25	100	pA
			70°C			4	nA
I_{IB}	Input bias current \ddagger	$V_{IC} = 0$	25°C		50	200	pA
			70°C			8	nA
V_{ICR}	Common-mode input voltage range			± 11	-12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10 \text{ k}\Omega$		± 12	± 13.5		V
A_{VD}	Large-signal differential voltage	$V_O = \pm 10 \text{ V}, R_L = 2 \text{ k}\Omega$	25°C		25	100	V/mV
			Full range			15	
r_i	Input resistance	$T_J = 25^\circ\text{C}$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$R_S \leq 10 \text{ k}\Omega$		70	100		dB
kSVR	Supply-voltage rejection ratio	See Note 2		70	100		dB
I_{CC}	Supply current				3.6	6.5	mA

\dagger Full range is 0°C to 70°C.

\ddagger Input bias currents of a FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as possible.

NOTE 2: Supply-voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously.

operating characteristics, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{O1}/V_{O2}	Crosstalk attenuation	$f = 1 \text{ kHz}$		120		dB
SR	Slew rate		8	13		V/ μs
B_1	Unity-gain bandwidth			3		MHz
V_n	Equivalent input noise voltage	$f = 1 \text{ kHz}, R_S = 20 \Omega$		18		$\text{nV}/\sqrt{\text{Hz}}$
I_n	Equivalent input noise current	$f = 1 \text{ kHz}$		0.01		$\text{pA}/\sqrt{\text{Hz}}$



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
LF353D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LF353P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
LF353PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

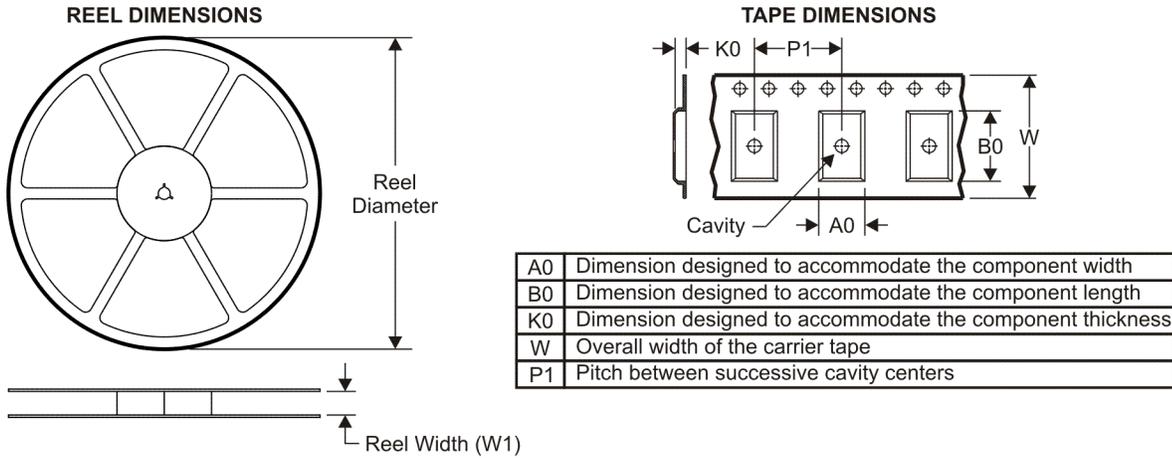
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

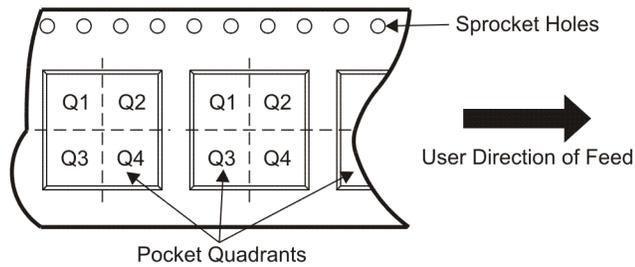
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TAPE AND REEL INFORMATION



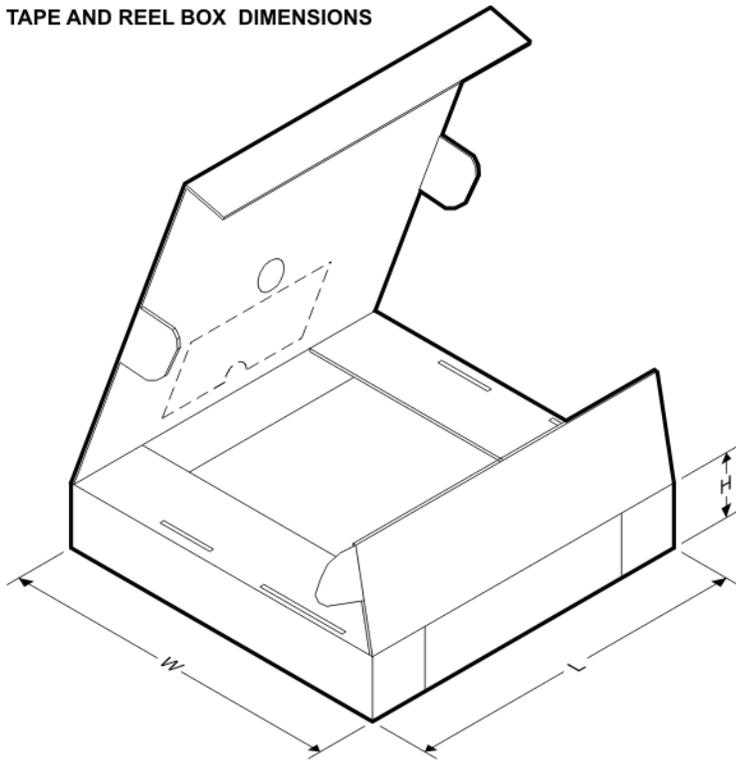
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LF353DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LF353DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

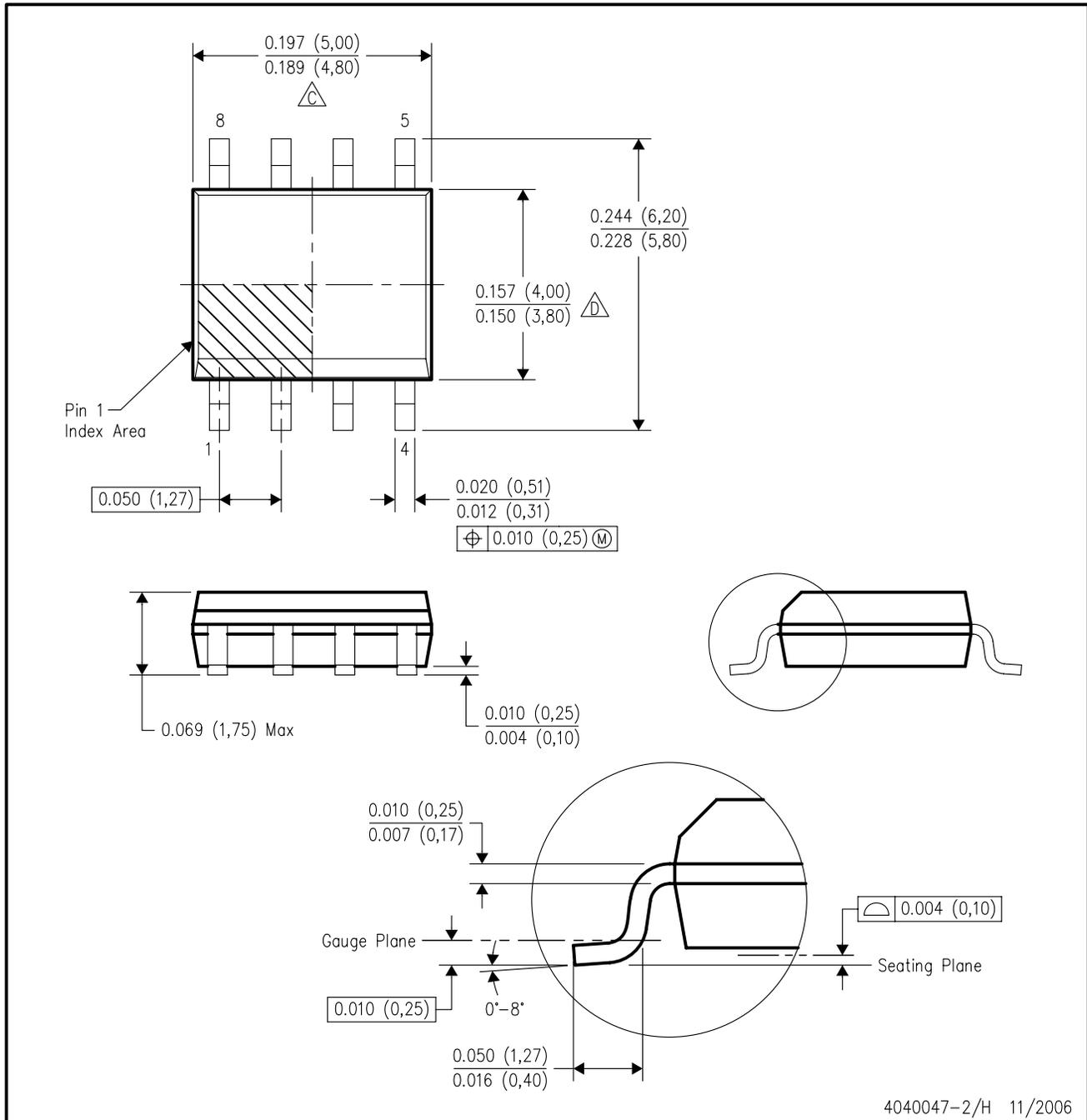


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LF353DR	SOIC	D	8	2500	346.0	346.0	29.0
LF353DR	SOIC	D	8	2500	340.5	338.1	20.6

D (R-PDSO-G8)

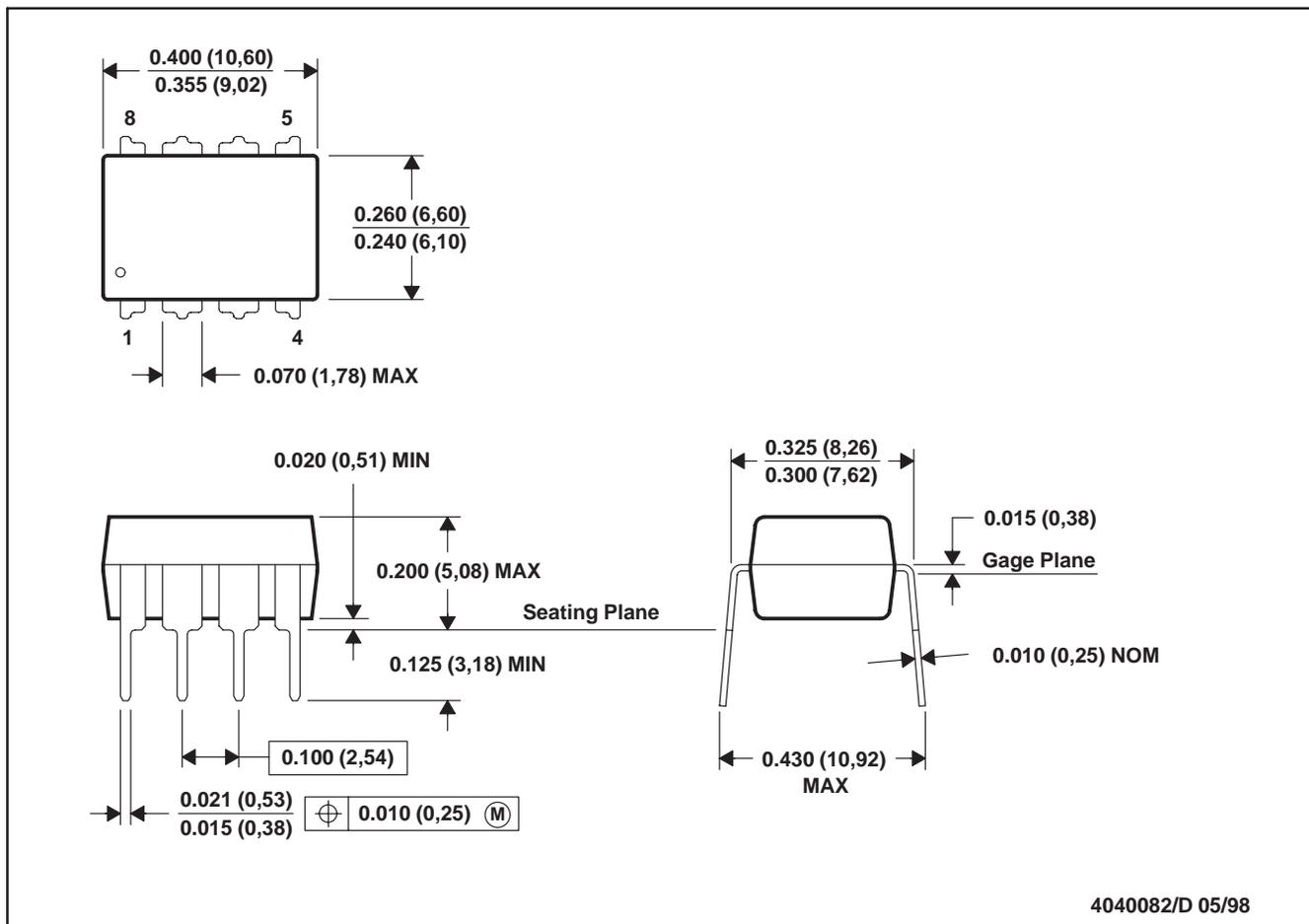
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

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